Massachusetts Institute of Technology | **Microsystems Research Center** | Cambridge Massachusetts 02139 | Room 39-321 Telephone (617) 253-8138

May 5, 1988

Dr. Clifford Lau
ONR Detachment
1030 East Green Street
Pasadena, CA 91106

Dear Clifford:

I am pleased to submit this "end-of-the-fiscal-year" letter report, for the period ending September 30, 1987.

1. CONTRACT TITLE

A COHERENT VLSI DESIGN ENVIRONMENT

ONR Contract Number: N00014-80-C-0622
ONR Work Unit Number: NR 622-013
Principal Investigator: Paul Penfield, Jr.
ONR Scientific Officer: Dr. Clifford Lau

2. BRIEF DESCRIPTIVE SUMMARY

This contract is terminating as of December 31, 1987, and the work has virtually finished by September 30, 1987. Work still to be completed will be reported under another contract, which started September 1, 1987, entitled "Critical Problems in Very Large Scale Computer Systems."

This work deals with VLSI CAD, Circuits, Architecture, and Theory.

The CAD effort is centered on timing analysis and circuit simulation. Advances have been made in tightening the bounds of timing analysis. The superiority of the Gauss-Jacobi technique for matrix solution, over the Gauss-Seidel method, has been proven when the algorithms are implemented on massively parallel machines.

In the circuits area, one result of importance is a new technique for calculating the highest frequency of operation of transistors with parasitic elements present. Work on a synthesis technique is under way.

In the architecture area, many new results have been derived for parallel algorithms and complexity. One of the most astonishing is that a hypercube with a large number of faulty nodes can be used, with high probability, as another perfectly functioning hypercube of half the size, by using reconfiguration algorithms that are simple, fast, and require only local information. Also, the design of the message-driven processor is continuing, with several advances in architecture, software, communications, and ALU design. Many of these are being implemented in VLSI circuits.

The theory work has as a central theme that the cost of communication should be included in complexity analyses. This has led to advances in models for computation, including volume-universal networks, routing, network flow, fault avoidance, queue management, and network simulation.

3. SIGNIFICANCE OF WORK

Much of the American research being carried out in computer architecture is divorced from activity in electrical networks and therefore does not naturally make use of realistic models. In particular, the cost of communication is frequently ignored in theoretical calculations. In our work, realistic cost models including communication are used. The result is a new body of knowledge that is more relevant to finding the ultimate limits on computation using real circuits.

The message-driven processor is a new architecture that employs message passing as an efficient communication and computation strategy. It is believed that massively parallel machines will be difficult if not impossible to program without a new methodology such as this one.

The new technique for finding the maximum frequency of operation of transistors with parasitics will enable vastly more complex models to be evaluated and will be useful for model generation and simplification. The work on waveform bounding has already led to fast algorithms for timing analysis, and the recent work will make such analysis even more accurate.

4. PUBLICATIONS

S. Bhatt, F. Chung, T. Leighton, and A. Rosenberg, "Optimal Simulations of Tree Machines," Proc. 27th IEEE Conference on Foundations of Computer Science, Portland, OR, October, 1986, pp. 274-282. Also, MIT VLSI Memo No. 86-354, December 1986.

R. E. Zippel, P. Penfield, Jr., L. A. Glasser, C. E. Leiserson, J. L. Wyatt, Jr., F. T. Leighton, and J. Allen, "Recent Results in VLSI CAD at MIT," Proc. 1986 Fall Joint Computer Conference, Dallas, TX, November 2-4, 1986, pp. 871-877. Also, MIT VLSI Memo No. 86-341, October 1986.

T. S. Hohol and L. A. Glasser, "RELIC: A Reliability Simulator for Integrated Circuits," Proceedings, International Conference on Computer-Aided Design, Santa Clara, CA, November 11-13, 1986. To appear (translated into Japanese) in Nikkei Microdevices. Also, MIT VLSI Memo No. 87-360, January 1987.

F. Chung, T. Leighton, and A. Rosenberg, "Embedding Graphs in Books: A Layout Problem with Applications to VLSI Design," SIAM J. Algebraic and Discrete Methods, vol. 8, no. 1, Jan. 1987, pp. 33-58. Also, MIT VLSI Memo No. 85-235, March 1985.

A. V. Goldberg, Efficient Graph Algorithms for Sequential and Parallel Computers, Ph.D Thesis, Department of Electrical Engineering and Computer Science, MIT, Cambridge, MA, February 1987. Also, Laboratory for Computer Science Technical Memorandum MIT-LCS-TR-374, February 1987.

C. W. Selvidge, A. C. Malamy, and L. A. Glasser, "Power and Communication Techniques for Physically Isolated Integrated Circuits," Proceedings, 1987 Conference on Advanced Research in VLSI, Stanford, CA, March 23-25, 1987, P. Losleben, ed., MIT Press, Cambridge, MA, 1987, pp. 231-247.

W. J. Dally, "Wire-Efficient VLSI Multiprocessor Communication Networks," Proceedings, 1987 Conference on Advanced Research in VLSI, Stanford, CA, March 23-25, 1987, P. Losleben, ed., MIT Press, Cambridge, MA, 1987, pp. 391-415.

L. A. Glasser, "Frequency Limitations in Circuits Composed of Linear Devices," to appear as "Frequency Limitations in Linear Circuits" in Proceedings, 1987 IEEE International Symposium on Circuits and Systems, Philadelphia, PA, May 4-7, 1987. Also, MIT VLSI Memo No. 86-348, November 1986.

J. Hastad, T. Leighton, and M. Newman, "Reconfiguring a Hypercube in the Presence of Faults," to appear in Proc. 1987 ACM Symposium on Theory of Computation.

A. V. Goldberg and S. A. Plotkin, "Parallel $(\Delta + 1)$ Coloring of Constant-Degree Graphs," to appear in Information Processing Letters.

A. V. Goldberg, S. Plotkin and G. Shannon, "Parallel Symmetry Breaking in Sparse Graphs," Proceedings, 19th Annual ACM Symposium on the Theory of Computing, New York City, NY, May 1987, pp. 315-324.

A. V. Goldberg and R. E. Tarjan, "Solving Minimum Cost Flow Problems by Successive Approximation," 19th Annual ACM Symposium on the Theory of Computing, New York City, NY, May 1987, pp. 7-18.

J. Hastad, T. Leighton and M. Newman, "Reconfiguring a Hypercube in the Presence of Faults," Proceedings, 19th Annual ACM Symposium on the Theory of Computing, May 1987, pp. 274-284.

Corey L. Kerstetter, Supplying Constant Current to Drive the Two-Phase Clocking of a VLSI Circuit, B.S. Thesis, Department of Electrical Engineering and Computer Science, May 1987.

J. Hastad, T. Leighton and B. Rogoff, "Analysis of Backoff Protocols for Multiple Access Channels," Proceedings, 19th Annual ACM Symposium on the Theory of Computing, May 1987, pp. 241-253.

John Burroughs, Reduction of Maximum Interconnect Length in Systolic Arrays, B.S. Thesis, Department of Electrical Engineering and Computer Science, June 1987.

W. J. Dally, L. Chao, A. Chien, S. Hassoun, W. Horwat, J. Kaplan, P. Song, B. Totty, and S. Wills, "Architecture of a Message-Driven Processor," Proceedings, 14th Annual Symposium on Computer Architecture, Pittsburgh, PA, June 2-5, 1987, pp. 189-196.

Toni Mari King, Automatic Generation of CMOS VLSI Clock Buffers, M.S. Thesis, Department of Electrical Engineering and Computer Science, June 1987.

Satish Rao, Finding Small Edge Separators in Planar Graphs, M.S. Thesis, Department of Elecrical Engineering and Computer Science, June 1987.

F. Miller Maley, Single-Layer Wire Routing, Ph.D. Dissertation, Technical Report MIT/LCS, TR-403, Laboratory for Computer Science, MIT, August 1987.

Guy E. Blelloch, "Scans as Primitive Parallel Operations," Proceedings, 1987 International Conference on Parallel Processing, St. Charles, IL, August 1987, pp. 355-362.

Thomas H. Cormen, "Efficient Multichip Partial Concentrator Switches," Proceedings, 1987 International Conference on Parallel Processing, St. Charles, IL, August 1987, pp. 525-532.

Adam Craig Malamy, A Magnetic Power and Communications Interface for Pinless Integrated Circuits, B.S. Thesis, Department of Electrical Engineering and Computer Science, MIT, September, 1987. Also MIT VLSI Memo No. 87-411, September 1987.

William J. Dally, "A Fine-Grain, Message-Passing Processing Node," Proceedings, 1987 Princeton Workshop on Algorithm, Architecture and Technology Issues for Models of Concurrent Computation, Princeton, NJ, September 30 - October 1, 1987.

William J. Dally and Paul Song, "Design of a Self-Timed VLSI Multicomputer Communication Controller, Proceedings, IEEE International Conference on Computer Design '87, Rye Brook, NY, October 5-8, 1987.

Joe Kilian, Shlomo Kipnis, and Charles Leiserson, "The Organization of Permutation Architectures with Bussed Interconnections," 28th Annual Symposium on Foundations of Computer Science, Marina Del Rey, CA, October 12-14, 1987, pp. 305-315.

S. Rao, "Finding Near-Optimal Separators in Planar Graphs," Proceedings, 1987 IEEE Symposium on Foundations of Computer Science, October 1987, pp. 225-237.

T. N. Bui, S. Chaudhuri, F. T. Leighton and M. Sipser, "Graph Bisection Algorithms With Good Average Case Behaviour," Combinatorica, vol. 7, no. 2, 1987, pp. 171-191.

A. Goldberg and S. Plotkin, "Parallel $\Delta + 1$ Coloring of Constant-degree Graphs," Information Processing Letters, vol. 25, no. 4, 1987.

R. M. Karp, F. T. Leighton, R. L. Rivest, C. D. Thompson, U. V. Vazirani and V. V. Vazirani, "Global Wire Routing in Two-Dimensional Arrays," Algorithmica, vol. 2, no. 2, 1987, pp. 113-129.

F. T. Leighton and P. Shor, "Tight Bounds for Minimax Grid Matching, with Applications to the Average Case Analysis of Algorithms," to appear in Combinatorica, 1988.

B. M. Maggs and S. A. Plotkin, "Minimum-cost Spanning Tree as a Path-finding Problem," Information Processing Letters, vol. 26, no. 6, 25 January 1988, pp. 291-293.

William J. Dally, "Performance Analysis of k-ary n-cube Interconnection Networks," to appear in IEEE Transactions on Computers.

Internal Memoranda

A. V. Goldberg and S. A. Plotkin, "Efficient Parallel Algorithms for $(\Delta + 1)$-Coloring and Maximal Independent Set Problems," Laboratory for Computer Science, MIT, Technical Memorandum MIT-LCS-TM-320, January 1987. Also MIT VLSI Memo No. 87-373, May 1987.

T. H. Cormen, "Efficient Multichip Partial Concentrator Switches," Laboratory for Computer Science, MIT, Technical Memorandum MIT-LCS-TM-322, February 1987. Also MIT VLSI Memo No. 87-372, April 1987.

J. L. Wyatt, Jr., "Nonlinear Dynamic Maximum Power Theorem," Research Laboratory of Electronics, MIT, RLE Technical Report No. 525, March 1987. Also MIT VLSI Memo No. 87-371, March 1987.

Andrew Vladislav Goldberg, "Efficient Graph Algorithms for Sequential and Parallel Computers," MIT VLSI Memo No. 87-378, May 1987.

Charles William Selvidge, "A Magnetic Communication Scheme for Integrated Circuits," MIT VLSI Memo No. 87-379, May 1987.

John L. Wyatt, Jr., "The Practical Engineer's No-Nonsense Guide to On-Chip Signal Delay Calculations," MIT VLSI Memo No. 87-381, May 1987.

S. N. Bhatt, F. R. K. Chung, J.-W. Hong, F. T. Leighton, and A. L. Rosenberg, "Optimal Simulations by Butterfly Networks," submitted to the 1988 ACM Symposium on Theory of Computing, October 7, 1987.

Lance A. Glasser, "Frequency Limitations in Circuits Composed of Linear Devices," MIT VLSI Memo No. 87-415, October 1987.

S. Malitz, "E-edge Graphs Have Pagenumber $O(\sqrt{E \log E})$," submitted to the 1988 ACM Symposium on Theory of Computing, November 2, 1987.

William J. Dally, "Concurrent Computer Architecture," MIT VLSI Memo No. 87-422, November 1987.

T. Leighton and E. Schwabe, "Space-Efficient Queue Management Using Fixed-Connection Networks," submitted to the 1988 ACM Symposium on Theory of Computing, November 1987.

Guy E. Blelloch and James J. Little, "Parallel Solutions to Geometric Problems on the Scan Model of Computation," MIT AI-Lab Technical Report TM-952, 1987.

Talks Without Proceedings

A. V. Goldberg, "A New Approach to the Maximum Flow Problem," MIT VLSI Research Review, Cambridge, MA, December 15, 1986.

J. Hastad, T. Leighton, and M. Newman, "Fault Tolerance in Hypercubes," MIT VLSI Research Review, Cambridge, MA, December 15, 1987.

J. Kilian, S. Kipnis, and C. E. Leiserson, "The Organization of Permutation Architectures with Multiple-Pin Interconnections," MIT VLSI Research Review, Cambridge, MA, December 15, 1986.

C. Selvidge and A. Malamy, "Magnetostatic I/O Techniques for Integrated Circuits," MIT VLSI Research Review, Cambridge, MA, December 15, 1986.

J. L. Wyatt, Jr., "Recent Progress on Delay Bounds for MOS Interconnect," Digital Equipment Corporation, Hudson, MA, December 1986.

F. T. Leighton, "Networks, Parallel Computation and VLSI Design," AMS/MAA National Meeting, January 1987.

F. T. Leighton, "Simulating Special-Purpose Networks with General-Purpose Networks," MIT LIDS Workshop on Distributed Computing, Cambridge, MA, January 1987.

F. T. Leighton, "Some Computational Properties of the Hypercube," BBN, Cambridge, MA, March 1987.

F. T. Leighton, "Some Computational Properties of the Hypercube," Princeton Workshop on Algorithms, Princeton, NJ, March 1987.

J. L. Wyatt, Jr., "Tellegen's Theorem -- What It Says, Why It's True, and Some of the Things It Predicts," Department of Computer Science, California Institute of Technology, Pasadena, CA, March 1987.

F. T. Leighton, "Some Computational Properties of the Hypercube," Princeton Workshop on Algorithms, April 1987.

F. T. Leighton, "Networks, Parallel Computation, and VLSI Design," Cornell University, Ithaca, NY, April 1987.

F. T. Leighton, "Networks, Parallel Computation, and VLSI Design," University of Cincinnati, Cincinnati, OH, April 1987.

F. T. Leighton, "Reconfiguring Networks Around Faults," Cornell University, Ithaca, NY, April 1987.

F. T. Leighton, "Some Computational Properties of the Hypercube," Cornell University, Ithaca, NY, April 1987.

T. H. Cormen, "Efficient Multichip Partial Concentrator Switches," MIT VLSI Research Review, Cambridge, MA, May 18, 1987.

W. J. Dally, L. Chao, A. Chien, S. Hassoun, W. Horwat, J. Kaplan, P. Song, B. Totty, and S. Wills, "Architecture of a Message-Driven Processor," MIT VLSI Research Review, Cambridge, MA, May 18, 1987.

L. A. Glasser and J. L. Wyatt, Jr., "Frequency Limitations in Circuits Composed of Linear Devices," MIT VLSI Research Review, Cambridge, MA, May 18, 1987.

P. O'Brien, J. L. Wyatt, Jr., T. Savarino, and J. Pierce, "Fast On-Chip Delay Estimation for Cell-based Emitter Coupled Logic," MIT VLSI Research Review, Cambridge, MA, May 18, 1987.

S. A. Plotkin and A. V. Goldberg, "Parallel Symmetry-breaking in Sparse Graphs," MIT VLSI Research Review, Cambridge, MA, May 18, 1987.

F. T. Leighton, "Analysis of Backoff Protocols for Multiple Access Channels," MIT LCS Annual Meeting, Cambridge, MA, June 1987.

F. T. Leighton, "Some Computational Properties of the Hypercube," IBM Watson Research Center, Yorktown Heights, NY, October 1987.

5. RESEARCH SUPPORT OF PAUL PENFIELD, JR.

5% Fall Term 1986; 5% Spring Term 1987; 25% Fall Term 1987
A Coherent VLSI Design Environment
Defense Advanced Research Projects Agency
Principal Investigator
$5,433,039 for the period July 1, 1984 to June 30, 1987

45% Academic; 100% Summer
Computer-Aided Fabrication System Implementation
Defense Advanced Research Projects Agency
Principal Investigator
$2,584,251 for the period April 1, 1985 to March 31, 1988

6. HONORS AND AWARDS

Guy Blelloch received the Outstanding Paper Award at the 1987 International Conference on Parallel Processing, for his paper entitled, "Scans as Primitive Parallel Operations."

Tom Cormen received the Distinguished Presentation Award at the 1987 International Conference on Parallel Processing for his paper entitled, "Efficient Multichip Partial Concentrator Switches."

The Fannie and John Hertz Foundation renewed Ron Greenberg's fellowship for 1987-1988.

F. Miller Maley was awarded a Postdoctoral Fellowship by the National Science Foundation for the years 1987-1989.

Cynthia A. Phillips was awarded an IBM Graduate Fellowship for 1987-1988.

7. PARTICIPANTS

FACULTY

Paul Penfield, Jr.
Jacob K. White
John L. Wyatt, Jr.
Thomas F. Knight, Jr.
Lance A. Glasser
William J. Dally
Charles E. Leiserson
F. Thomson Leighton

STUDENTS

Mark Reichelt
Waldemar Horwat
Paul Song
Andrew Chien
Serge Plotkin
Joel Wein
Jeffrey Mark Siskind
Jerry Larivee
Guy Blelloch
Stuart Fiske

Mark Newman
Shlomo Kipnis
Jeff Fried
Tom Cormen
Bruce Maggs
Ron Greenberg
James Park
Alex Ishii
Cindy Phillips
Eric Schwabe
Dina Kravets
Seth Malitz

Soho N. M. Hassoun
Jonathan D. Sieber
Margaret St. Pierre
Steven Weiner
Feng Zhao
Sui-Ling Ku
Peter Osler
Satish B. Rao
Steven Seda
Lisa Melcher
Carl Hoffman

STAFF

John T. Wroclawski

8. DEGREES GRANTED TO STUDENT PARTICIPANTS

Adam Craig Malamy, A Magnetic Power and Communications Interface for Pinless Integrated Circuits, B.S. Thesis, Department of Electrical Engineering and Computer Science, MIT, September, 1987. Also MIT VLSI Memo No. 87-411.

A. V. Goldberg, *Efficient Graph Algorithms for Sequential and Parallel Computers*, Ph.D Thesis, Department of Electrical Engineering and Computer Science, MIT, Cambridge, MA, February 1987. Also, Laboratory for Computer Science Technical Memorandum MIT-LCS-TR-374, February 1987.

Corey L. Kerstetter, Supplying Constant Current to Drive the Two-Phase Clocking of a VLSI Circuit, B.S. Thesis, Department of Electrical Engineering and Computer Science, May 1987.

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Satish Rao, Finding Small Edge Separators in Planar Graphs, M.S. Thesis, Department of Electrical Engineering and Computer Science, June 1987.

F. Miller Maley, Single-Layer Wire Routing, Ph.D. Dissertation, Technical Report MIT/LCS, TR-403, Laboratory for Computer Science, MIT, August 1987.

Sincerely,

Paul Penfield, Jr.
Professor of Electrical
Engineering